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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/811,444	03/20/2001	Takashi Kobayashi	500.39879X00	9563

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EXAMINER	
QUINTO, KEVIN V	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/31/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/811,444	KOBAYASHI, TAKASHI	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7 and 14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 7 and 14 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti et al. (USPN 6,410,387 B1) in view of Shum et al. (USPN 6,327,182 B1) and further in view of He et al. (USPN 6,143,608).

4. In reference to claim 7, Cappelletti et al. (USPN 6,410,387 B1, hereinafter referred to as the "Cappelletti" reference) discloses a similar device. Figure 20 discloses a nonvolatile semiconductor memory device. The memory cell region is in the middle of this figure and has a first MOS field effect transistor, a floating gate (7), and a control gate (29). It is understood that what is shown is one unit cell of a memory cell array comprising a plurality of memory cells arranged as a matrix. The memory cell region in the device of Cappelletti does not have its own dedicated well within the substrate. However a nonvolatile semiconductor device having a memory cell portion

which uses its own dedicated well is well known in the art. Shum et al. (USPN 6,327,182 B1, hereinafter referred to as the "Shum" reference) discloses a nonvolatile semiconductor device in figure 9 which uses a memory cell portion that has its own well within the substrate. Shum further discloses (in column 5, lines 28-40) that a memory cell portion which is in a separate well "allows biasing during operation of the memory cells with a reduced likelihood of disturbing non-selected memory cells." It would therefore be obvious to use a separate well for the memory cell portion in the device of Cappelletti in order to avoid disturbing non-selected memory cells. Thus in the device of Cappelletti constructed in view of Shum, there is a floating gate (7) and control gate (29) formed on a well. There is a first diffusion layer which function as a source (30) and a drain (31). There is a tunnel dielectric film (5) between the well and the floating gate (7). There is also an interpoly dielectric film (18) between the floating gate (7) and the control gate (29). Figure 20 of Cappelletti also shows a peripheral circuit region to the right of the memory cell region. Within the peripheral circuit region, there is a second MOS field effect transistor which has a second well (21) formed in the substrate (1). There is a second diffusion layer formed in the second well (21) which functions as a source (44) and a drain (45). There is a gate electrode (26) which is formed on the second well (21) with the interposition of a gate insulating film (24). This gate insulating film (24) is also the first insulating film which is deposited on the semiconductor substrate (1). It is also understood that there is a plurality of these second MOS field effect transistors. As can be seen in the figure, shallow groove or trench isolation is utilized for isolation of the second MOS field effect transistors. The first insulating film

(24) of Cappelletti is understood to be silicon oxide (column 5, line 1). It is also understood that the first oxide layer of the interpoly dielectric or the second insulating film (24) is silicon oxide. Cappelletti discloses that the interpoly dielectric film is made of three deposited layers (oxide-nitride-oxide, column 4, lines 24-25). The first such oxide meets the claim limitation, "a second deposited insulating film." Cappelletti and Shum teach all of the claimed invention except for the exact thickness of the second deposited insulating film. Although Cappelletti and Shum do not teach the exact thickness as that claimed by Applicant:

> **The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Leshin, 125 USPQ 416.**

Therefore this limitation is not patentably distinguishable over the Cappelletti and Shum references. Neither Cappelletti nor Shum discloses the use of nitrogen in the gate insulating film of the second MOS field effect transistor. However the use of nitridation in the formation of nonvolatile memory and peripheral circuitry is well known in the art. He et al. discloses a peripheral transistor gate insulating film which receives a lower nitridation concentration (column 11, lines 56-62) than the second insulating film within the interpoly dielectric. It is understood that the second insulating film contains a high nitrogen concentration since it undergoes nitridation to enhance the tunnel oxide (the second insulating film) reliability (column 2, lines 1-9).

5. In reference to claim 14, Cappelletti et al. discloses a similar device. Figure 20 discloses a nonvolatile semiconductor memory device. The memory cell region is in the middle of this figure and has a first MOS field effect transistor, a floating gate (7), and a

control gate (29). It is understood that what is shown is one unit cell of a memory cell array comprising a plurality of memory cells arranged as a matrix. The memory cell region in the device of Cappelletti does not have its own dedicated well within the substrate. However a nonvolatile semiconductor device having a memory cell portion which uses its own dedicated well is well known in the art. Shum et al. (USPN 6,327,182 B1, hereinafter referred to as the "Shum" reference) discloses a nonvolatile semiconductor device in figure 9 which uses a memory cell portion that has its own well within the substrate. Shum further discloses (in column 5, lines 28-40) that a memory cell portion which is in a separate well "allows biasing during operation of the memory cells with a reduced likelihood of disturbing non-selected memory cells." It would therefore be obvious to use a separate well for the memory cell portion in the device of Cappelletti in order to avoid disturbing non-selected memory cells. Thus in the device of Cappelletti constructed in view of Shum, there is a floating gate (7) and control gate (29) formed on a well. There is a first diffusion layer which function as a source (30) and a drain (31). There is a tunnel dielectric film (5) between the well and the floating gate (7). There is also an interpoly dielectric film (18) between the floating gate (7) and the control gate (29). Figure 20 of Cappelletti also shows a peripheral circuit region to the left and right of the memory cell region. Within the peripheral circuit region, there is a second MOS field effect transistor which has a second well (21) formed in the substrate (1). There is a second diffusion layer formed in the second well (21) which functions as a source (44) and a drain (45). There is a gate electrode (26) which is formed on the second well (21) with the interposition of a first gate insulating film (24). It

is understood that there is a plurality of these second MOS field effect transistors. There is a third MOS field effect transistor which has a third well (15) formed in the substrate (1). There is a third diffusion layer formed in the third well (15) which functions as a source (16) and a drain (17). There is a second gate electrode (8) which is formed on the third well (21) with the interposition of a second gate insulating film (3). This second gate insulating film (3) is thicker than the first insulating film (24). As can be seen in the figure, shallow groove or trench isolation is utilized for isolation of the peripheral circuit region. The first insulating film (24) of Cappelletti is understood to be silicon oxide (column 5, line 1). It is also understood that the first oxide layer of the interpoly dielectric or the second insulating film (24) is silicon oxide. Cappelletti discloses that the interpoly dielectric film is made of three deposited layers (oxide-nitride-oxide, column 4, lines 24-25). The first such oxide meets the claim limitation, "a second deposited insulating film." Cappelletti and Shum teach all of the claimed invention except for the exact thickness of the second deposited insulating film. Although Cappelletti and Shum do not teach the exact thickness as that claimed by Applicant:

> The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Leshin, 125 USPQ 416.

Therefore this limitation is not patentably distinguishable over the Cappelletti and Shum references. Neither Cappelletti nor Shum discloses the use of nitrogen in the gate insulating film of the second MOS field effect transistor. However the use of nitridation in the formation of nonvolatile memory and peripheral circuitry is well known in the art.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ
March 24, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800